

PATENT APPLICATION TRANSMITTAL SHEET

Customer No. 20350

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(650) 326-2400

Attorney Docket No.: 15114-052310

"Express Mail" Label No. EL525625496US

Date of Deposit: March 2, 2000



BOX PATENT APPLICATION

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Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is the

- ☒ patent application of
- ☐ continuation patent application of
- ☐ divisional patent application of
- ☐ continuation-in-part patent application of

Date: March 2, 2000

By: [Signature]

Inventor(s)/Applicant Identifier: Sidney Larry Anderson et al.

For: METHOD AND STRUCTURE FOR INTEGRATED CIRCUIT PACKAGE

☒ This application claims priority from each of the following Application Nos./filing dates:
U.S. Provisional Patent Application No. 60/123,116, filed March 5, 1999 & U.S. Provisional Patent Application No. 60/126,234, filed March 24, 1999, the disclosures of which are incorporated by reference.

Enclosed are:

- ☒ Title Page.
- ☒ Thirteen (13) pages of specification.
- ☒ Six (6) pages of claims.
- ☒ One (1) page of Abstract.
- ☒ Eight (8) sheets of ☐ formal ☒ informal drawings.
- A ☒ signed ☐ unsigned Declaration.
- A ☒ signed ☐ unsigned Power of Attorney by Assignee.
- A ☒ signed ☐ unsigned Assignment of the invention to Altera Corporation.
- Information Disclosure Statement Under 37 C.F.R. §1.97, Form PTO-1449, & one (1) cited reference.

	(Col. 1)	(Col. 2)	
FOR:	NO. FILED	NO. EXTRA	
BASIC FEE			
TOTAL CLAIMS	48 - 20	= 28	
INDEP. CLAIMS	8 - 3	= 5	
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENTED			

* If the difference in Col. 1 is less than 0, enter "0" in Col. 2.

SMALL ENTITY	
RATE	FEE
	\$345.00
x \$9.00 =	
x \$39.00 =	
+ \$130.00 =	
TOTAL	

OTHER THAN SMALL ENTITY	
RATE	FEE
	\$690.00
x \$18.00 =	\$504.00
x \$78.00 =	\$390.00
+ \$260.00 =	\$0.00
TOTAL	\$1,584.00

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- ☒ Filing fee \$1,584.00
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Telephone:
(650) 326-2400

Facsimile:
(650) 326-2422

Respectfully submitted,
TOWNSEND and TOWNSEND and CREW LLP

Craig P. Wong
Craig P. Wong
Reg. No.: 45,231
Attorneys for Applicant

PATENT

Attorney Docket No.: 015114-052310US

Client Reference No.: A515

PATENT APPLICATION

**METHOD AND STRUCTURE FOR INTEGRATED CIRCUIT
PACKAGE**

Inventor(s):

Sidney Larry Anderson
42991 Luzon Drive
Fremont, CA 94539
a citizen of United States

Jon Long
256 Helen Way
Livermore, CA 94550
a citizen of United States

Donald S. Fritz
5105 Southwick Court
San Jose, CA 95136
a citizen of United States

Assignee:

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
A Delaware Corporation

Entity: Large

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400

METHOD AND STRUCTURE FOR INTEGRATED CIRCUIT

PACKAGE

The application claims priority to U.S. Provisional Application 60/123,116, filed March 5, 1999, and U.S. Provisional Application Number 60/126,234, filed March 24, 1999, and is related to U.S. Nonprovisional Application No. ____/_____, filed _____ (Attorney Docket Number 015114-052410US), which are incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to the field of integrated circuit technology, and more specifically to techniques of packaging integrated circuits.

Integrated circuits (ICs) or "chips" are becoming denser and are providing higher performance and functionality per unit area. Many ICs have hundreds of pads that will interface with the printed circuit board (PCB). The packaging for the IC connects the pads of the chip to the pins, leads, or other electrical contacts of the package.

It is important that the IC package is relatively low in cost. Previous generations of IC packages were ceramic or included materials or used techniques that increased the cost of the packaging. It is also important that the IC packaging sufficiently protect the chip and provide the necessary number of electrical connections (e.g., leads), and provide this function using as small a package size as possible. A package with a smaller footprint takes up less PCB space and more ICs can be mounted on a single PCB.

Another important consideration in IC packaging is reliability. One concern is that when an IC package is soldered to the PCB, the IC package should be reliably electrically connected to the PCB, or else over time open circuit or no connection failures will result. Because temperature cycling occurs when the IC heats up during operation and cools off during non-operation, the solder ball connections between the IC and the PCB may be subjected to shear and stress forces due to the package expansion and contraction. The solder balls may work harden and then fracture. Cracks in the solder balls will cause open circuits, which inevitably leads to system failure. Consequently, it is quite important to design the IC package so that the temperature cycling does not cause premature solder joint and system failure.

Therefore, as can be appreciated, methods and devices are needed to provide IC packaging with a lower cost, smaller package size, and better reliability. Specifically, there is a need to design integrated circuit packages which enhance solder ball reliability and longevity while maintain the small size of the package and large amount of contacts between the die and the PCB.

SUMMARY OF THE INVENTION

The present invention provides a stress relief buffer zone between the die and the solder ball array which absorbs the mechanical and thermal stress from temperature cycling. A transition medium relieves the stress above and below the die and acts as the stress buffer zone. The transition medium also moves the die towards the center of the packaging and allows the molding compound and transition medium to expand and contract while keeping the die relatively motionless. By moving the die towards the middle of the packaging, the transition medium reduces the warpage and curling of the package. The reduction of the warpage and curling increases the life of the solder ball joint, and accordingly increases the life of the electronic device. The transition medium is typically composed of a stress absorbent material, and has a CTE similar to the mold compound, the PCB, or both.

In a first aspect, the present invention provides an integrated circuit package comprising a silicon die having a first thickness and a metallized polymer layer having a first and second side. A transition medium is disposed between the silicon die and the first side of the metallized polymer layer. The transition medium has a second thickness which is greater than the first thickness of the silicon die.

In another aspect, the present invention provides an integrated circuit package comprising a metallized polymer layer defining a first thickness. A transition medium is coupled to the metallized polymer layer. A die is coupled to the transition medium. A mold cap encapsulates the transition medium and the die. The mold cap defines a second thickness, such that the first thickness of the metallized polymer layer and the second thickness of the mold cap define a package thickness. The die is disposed near the middle of the package thickness.

In yet another aspect, the present invention provides an integrated circuit comprising a first adhesive layer with a coefficient of thermal expansion disposed on a tape carrier. A transition medium having a first and second surface is mounted on the first adhesive layer such that the first surface of the transition medium engages the first

adhesive layer. A second adhesive layer is disposed on the second surface of the transition medium and a die is disposed on the second adhesive layer. A mold cap encapsulates the first adhesive layer, the transition medium, the second adhesive layer, and the die. The mold cap and tape carrier define a package thickness. The coefficient of thermal expansion of the transition medium and the mold cap have approximately the same coefficient of thermal expansion so as to reduce the thermal stress on the die during thermal cycling.

In a further aspect, the present invention provides a method of packaging an integrated circuit. The method comprises providing a silicon die adhered to a rigid transition medium. A layer of adhesive is applied to a tape carrier. The die and transition medium are mounted to the adhesive on the tape carrier. The die and transition medium are then encapsulated.

In yet another aspect, the present invention provides a method of forming an integrated circuit package. The method comprises providing a metallized polymer layer. A rigid transition medium layer is attached to the metallized polymer layer through a first adhesive layer. An integrated circuit is coupled to the rigid transition medium using a second adhesive layer.

In yet another aspect, the present invention provides a method of fabricating an integrated circuit. The method comprises providing a semiconductor wafer. The semiconductor wafer is attached to a transition medium using a first adhesive. A die is cut from the semiconductor wafer, wherein the die is attached to a corresponding area of the transition medium. The die and transition medium are mounted to a tape carrier.

In yet another aspect, the present invention provides a method of forming an integrated circuit package comprising providing a tape carrier and a silicon die. The thermal mismatch stress between the die and the integrated circuit package is reduced by disposing a rigid transition medium between the tape carrier and the silicon die.

Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings, in which like reference designations represent like features throughout the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of an integrated circuit package;

Figure 2 is an exploded view taken from Figure 1;

Figure 3 is a cross sectional view of a BGA package with a die near the bottom of the packaging;

Figure 4 illustrates the warpage and curling of the BGA package due to the temperature differentials of the package components;

Figure 5 is a cross-sectional view of an integrated circuit package according to one embodiment of the present invention;

Figure 6 is an exploded view taken from Figure 5;

Figure 7 is a cross sectional view of a integrated circuit package having a die near the center of the package;

Figure 8 is a top-view of a chip package according to the embodiment shown in Figure 5;

Figures 9A to 9F illustrate a method of the present invention;

Figures 10A to 10E illustrate another method of the present invention;

Figures 11A to 11F illustrate yet another method of the present invention;

and

Figures 12A to 12C illustrates another method of the present invention.

DETAILED DESCRIPTION

Figure 1 shows a cross-sectional view of an integrated circuit (IC) package 12. The package is a ball grid array (BGA) package. The pins or leads for the package are solder balls 14 arranged in a grid or array pattern on the underside of the package. The package is typically surface mounted on a PC board 16 using solder balls 14. BGA packages can accommodate higher numbers of I/O pins because a greater numbers of solder ball leads 14 can be placed in a grid array pattern underneath the package. For example, some BGA packages have 672 or more solder ball leads 14, while PLCC packages are often limited to 304 leads.

It is understood that although the present invention will be described in relation to the BGA package types, the present invention is applicable to package types other than the BGA type. The present invention is applicable to any package which has electrical leads which are subject to stress. In fact, as the semiconductor continues to advance, there will undoubtedly be new package types that do not yet exist or have not yet become standardized. The principles of the present invention will also be applicable to the new package types as well.

Many types of integrated circuits are being designed to have greater numbers of I/O pins. Microprocessors, ASICs, PLDs, and FPGAs generally can have high I/O pin counts. For example, the Altera Fine Line BGA package has 672 pins. Some examples of products using BGA packages include Altera's 10K family of Fine Line™ and SameFrame™ products. The terms “solder ball,” “lead,” and “pin” are used interchangeably throughout the specification and are used to signify electrical contact points between the IC package and a substrate such as a printed circuit board (PCB).

BGA packages will have a better lead density (pins per square inch) and support a greater number of input/output (I/O) pins than other PLCC, QFP, and PGA packages of the same size. The areas of the BGA package typically has an area of 11 square millimeters, 17 square millimeters, 23 square millimeters, 27 square millimeters, 35 square millimeters, 45 square millimeters, or larger package sizes. Naturally, it will be appreciated that the package size will vary depending on the function of the chip and the electronic device. It is expected that the solder ball count of the BGA packages will increase since the trend is to produce even more highly integrated circuitry. This is especially true for ICs such as microprocessors, ASICs, and CPLDs. Such large numbers of solder balls will provide electrical connections between a PCB and an ever increasing number of I/O pins. BGA packages can have 100, 256, 484, 672, 2000, or more solder balls.

Figure 1 illustrates a BGA package 12 comprising a silicon die 18 mounted to a metallized polymer tape 20 through a die attach 22. Metallized polymer tape 20 comprises traces that route each pad 24 of die 18 to appropriate solder ball landing areas. Metal wires 26 electrically connect die 18 to solder balls 14 through the etched circuit leads to electrically connect the chip to the PC board. Die 18 and metal wires 26 are encased or encapsulated using mold cap 28, to protect the semiconductor die and package components from various stresses such as temperature stress and mechanical stress. A thickness 30 of package 12 is approximately 0.060 inches. A thickness 32 of package 12, including solder balls 14, is approximately 0.073 inches. A width 34 of a solder ball 14 is approximately 0.019 inches. Naturally, the package dimensions can vary depending on the size of the silicon die 18, the number of I/O pins, the number and size of the solder balls 14, and similar factors.

Figure 2 shows an exploded view of section 11 of Figure 1. Silicon die 18 contains electronic circuitry. Some examples of IC chips include microprocessors, programmable logic, ASICs, DSPs, and broadband ICs. Die 18 can be made of materials

other than silicon such as gallium arsenide, or the like. Input/output bonding wires 26 are electronically coupled to pads 24 of die 18 at appropriate locations on tape carrier 20. Bonding wires 26 can be composed of conducting materials, such as aluminum, gold, copper, silver, or the like. Die 18 is attached to tape carrier 20 using an adhesive or die attach 22. Die attach 22 can be one of many materials that can sufficiently bond die 18 to tape carrier 20. For example, die attach materials can include latex cements; thermosetting adhesives such as epoxies, cyanoacrylates, acrylics, and polyesters; thermoplastic adhesives such as polyesters, polyvinyl acetals, acrylics, and polyamides; cellulose acetates; elastomer adhesives such as urethanes, silicones, neoprecor, and natural rubbers; and alloy adhesives such as epoxy-nylons, epoxy polysulfides, and vinyl phenolics.

The BGA package employs a tape package construction that provides greater flexibility for routing die-to-package terminations. In a BGA package, the bonding wires electrically couple the pads of the die to pads or traces on the tape carrier. This tape carrier has traces (like a PC board) that routes each pad of the die to appropriate solder ball landing area. Therefore, by changing the traces of the tape carrier, the routability to solder ball connections underneath the die can be flexibly changed. This reduces the package size compared to PLCC and other package types. Current tape package technology typically supports twenty five micron traces within a twenty five micron space. The tape technology is about twice as effective as the closest competitive technology. The tape carrier is typically made on a continuous flexible printed circuit material with conducting traces, such as a polyimide film tape. These traces can be made of a conducting material such as copper, metallized polymer layers, or the like.

Table 1 lists typical dimensions of various package components.

TABLE 1

Package Component	Typical Dimensions
Mold cap	0.7 to 1.5 square millimeters
Bonding wires	0.8 to 1.3 (doped gold wire)
Silicon die	6 to 10 mils
Adhesive	2 to 4 mils
Solder balls	18 to 25 mils
Tape carrier	2 to 3 mils (w/ 1 mil metallization)

Despite the success of tape package construction, there are potential problems. One concern is the reliability of the solder ball joints between the BGA package and the PCB. Because a system is turned on and off, there is expansion and contraction of the BGA package and the PCB due to the temperature cycling. In particular, solder balls 14 experience shear stress due to the mismatched coefficients of thermal expansion (CTE) among the various components of the device. Such a problem arises, for example, when the CTE of the silicon die is sufficiently mismatched with the CTE of the PCB onto which the components are mounted. Such differences can be large. For example, the typical CTE of a die can be as low as $2.6 \times 10^{-6}/^{\circ}\text{C}$ and that of a PCB can be as high as $17 \times 10^{-6}/^{\circ}\text{C}$.

A problem stemming from the mismatched CTEs is IC package warpage or curling. Specifically, the IC package expands and shrinks more than the die. Figures 3 and 4 illustrate an integrated circuit package 12 coupled to PCB 16 with solder balls 14. Because of the symmetry of the packaging, expansion and shrinkage proceeds outward from the stationary central point 36 of the package. As shown in Figure 3 die 18 typically sits near the bottom of packaging 12. Because the CTE of the die is smaller than the CTE of plastic encapsulant 28, the bottom of the package does not expand and contract as much as the top of the package. As shown in Figure 4, this tends to pull the lower edges of the package upward and tends to curl package 12. This subjects the outermost solder balls to large shear and bending forces. Thus, the solder balls that typically fail first are

those that are positioned furthest away from the center of the IC package. The open connection from the cracked solder ball inevitably leads to a system failure.

Table 2 lists typical CTEs for various package components.

TABLE 2

Package Component	Typical CTEs ($1 \times 10^{-6}/^{\circ}\text{C}$)
Mold cap	7 to 15
Silicon die	2.6 to 6
Adhesive	58
Package substrate	12 to 17
Solder balls	24
Tape carrier	12
PCB	17

5 Larger packages tend to experience more failures than smaller packages because the larger packages experience more expansion than smaller packages. Consequently, the larger die sizes have a significant effect on solder ball joint reliability. For example, for die sizes less than 3 square millimeters, the number of failure-free cycles can be as high as 5000 cycles. The number of failure-free cycles, however, drop below
10 2000 cycles for die sizes greater than 5 square millimeters and down to 1000 cycles for die sizes greater than 10 square millimeters.

 One technique to improve solder ball reliability is using bigger and taller solder balls. Bigger solder ball increase the area of contact between the solder ball and the PCB and increase the life of the solder ball joint. One problem with bigger solder
15 balls is the limited space on the die packages. Bigger solder balls take up more space, and decrease the potential number of electrical contacts between the die and PCB.

 Taller solder balls increase the distance between the solder ball and the PCB, and allow more swing between the top and bottom of the solder ball. This can lower the contention at the solder ball joints. One problem with taller solder balls,

however, is they raise the overall height of the die package which is contrary to the goal of minimizing package sizes.

Figure 5 shows a cross-sectional view of an embodiment of the integrated circuit package 200 of the present invention. Similar to Figures 1 and 2, a thickness 30 of package 12, including tape carrier 20 and plastic encapsulant 28, is typically about 0.060 inches. A thickness 32 of package 12 with solder balls 14 is typically about 0.073 inches. A width 34 of a solder ball is typically about 0.019 inches. Naturally, the dimensions of the components of the package will change depending on factors such as the size of the die, the number of I/O pins, the number and size of the solder balls, and the like.

As shown most clearly in Figure 6, the integrated circuit package has a transition medium 42 between tape carrier 20 and the silicon die 18. A first adhesive 38 adheres transition medium 42 to tape carrier 20, and a second adhesive 40 adheres die 18 to transition medium 42. The active region of die 18 faces away from tape carrier 20. Bonding wires 26 couple pads or other features 24 of silicon die 18 to appropriate locations on the tape carrier. Naturally, it will be appreciated that the transition medium 42 can be coupled to silicon die 18 and tape carrier 20 using other conventional methods, such as transfer or injection molding.

The IC package in Figures 5 and 6 provides improved reliability with respect to mismatched CTE stress and die positioning. Transition medium 42 acts as a buffer and absorbs much of the stress at a solder ball joint 44 between package 12 and PCB 16. Transition medium 42 material should be rigid enough to support the die. The transition medium may include materials such as mold compound 28, BT resin, FR-4 resin, FR-5 resin, polymers, elastomer, adhesives, and the like. While it is possible to use nonpolymers such as a metal or silicon, it has been found that the above mentioned materials provide better stress absorption than the metals and silicon. All of these materials, however, are desirable because they have a CTE which is similar to the PCB, mold compound materials, or both. Transition medium 42 typically has a CTE between approximately $7 \times 10^{-6}/^{\circ}\text{C}$ and $17 \times 10^{-6}/^{\circ}\text{C}$, and preferably between $7 \times 10^{-6}/^{\circ}\text{C}$ and $12 \times 10^{-6}/^{\circ}\text{C}$. Such a CTE provides a similar CTE to the surrounding PCB and mold compound and provides a more uniform contraction and expansion of the die packaging 12.

Transition medium 42 positions the die closer to the middle of package thickness 30. Having the die 18 near the middle of the package thickness 30 reduces the problem of package warpage and curling. The top and the bottom of the package can

contract more equally and the forces on the die can be reduced. As shown in Figure 7, when mold compound 28 and transition medium 42 expand and contract, because the die is near the center, the die's movement will be minimized. Moreover, positioning the die 18 closer to the middle moves the die farther from the solder ball array and reduces the stress on the die 18. Accordingly, die 18 can be made thinner without jeopardizing its integrity. The die thickness can be reduced from 18 mils down to 1 mil or less by plasma etching, mechanical grinding, lapping, or the like. In a specific embodiment, the die is reduced to a thickness of 6 mils by plasma etching. Although other techniques are available, plasma etching is used because thickness down to about 2 mils may be obtained. Thus, in many embodiments die 18 is thinner than transition medium 42. Because the die is thinner, there is less die material and the thermal mismatch stress should be reduced.

Figure 8 shows a top view according to the embodiment shown in Figure 7. Specifically, Figure 8 illustrates the die 18, transition medium 42, and tape carrier 20. In the illustrated embodiment, the transition medium 42 length l_{tm} and width w_{tm} are at least as long and wide as the die 18 length l_d and width w_d . In other embodiments, the transition medium 42 can have a smaller or larger area than the die. The die and transition medium can be any number of shapes, including but not limited to circular, rectangular, square, or the like. While solder balls 14 can be positioned anywhere on the packages, in this embodiment, solder balls 14 are disposed underneath both the tape carrier 20 and die 18.

An integrated circuit package of the present invention may be formed in a number of ways and for use in a number of different applications. One method for producing the present invention is illustrated in Figures 9A to 9F. As shown in Figure 9A, a conventional tape carrier 50 having a patterned conductive layer and a dielectric layer having vias is typically mounted beneath a copper support frame 52 prior to processing. Any conventional two layer or three layer polyimide tape carrier can be used. A first layer of adhesive 54 can be applied to polyimide tape carrier 50 (Figure 9B). Any standard technique of applying the adhesive can be used. For example, a standard heat press technique, b stage (application and partial cure), or the like can be used. Before being attached to tape carrier 50, transition medium 56 can be precut to a size at least as large as the die that will be used. Transition medium 42 length l_{tm} and width w_{tm} should be at least as long and wide as die 58 length l_d and width w_d . (See Figure 8). As shown in Figure 9C, transition medium 56 is then mounted onto the first layer of adhesive 54. A

second layer of adhesive 60 is applied to the top surface of the transition medium 56 (Figure 9D). A die 58 is typically thinned by back lapping, polishing methods, plasma etching, or the like, prior to mounting on the second adhesive layer (Figure 9E). Bonding wires 62 can be attached to pads or other features of the die 58 to electrically connect the die to appropriate locations on tape carrier 50. Die 18 can then be encased or encapsulated using mold cap 64. (Figure 9F).

Solder balls or other conductive balls can thereafter be positioned to electrically connect the tape carrier electrical traces to the printed circuit board using any conventional method suitable for forming a secure electrical connection between the solder balls and the pads (not shown). For example, the solder balls may be added through solid or liquid deposition followed by infrared, convection, vapor phase, soldering, or the like.

The combination of the adhesive layers 54, 60, transition medium 56, and die 58, typically have a thickness between approximately 14 mils and 20 mils, and preferably approximately 18 mils. Naturally, the relative thicknesses can vary depending on materials, overall thickness of the package, and the type of device. In an exemplary embodiment, adhesive layers 54, 60 have a thickness of 2 mils, transition medium 56 has a thickness of approximately 10 mils and die has a thickness of approximately 6 mils. Typically, there is no bonding wire between the transition material and the die. The transition material need not be grounded for this invention to work well. Although the illustrated embodiments employ a single transition medium, it will be understood that more than one transition medium may be employed. For example multiple layers of materials having different CTEs or multiple layers of the material having the same CTE maybe by disposed between the die and the solder balls. Moreover, transition medium 56 may have gaps which allow the mold encapsulant to intervene in an area directly between die 58 and tape carrier 50.

Figures 10A to 10E illustrate an alternative method of producing the present invention. In particular, die 58 and transition medium 56 are adhered together prior to mounting on the tape carrier 50. As shown in Figures 10A and 10B, transition medium 56 is attached to die 58 with an adhesive layer 60 to form sandwich 66. A second adhesive layer 54 can be applied to a surface of tape 54 at the desired position. (Figure 10C). The sandwich 66 can then be attached to the second adhesive layer 54 (Figure 10D). Bonding wires 62 can be attached to the pads or other features of the die

58 to electrically connect die 58 to the tape carrier 50. Die 58 can then be encased or encapsulated using a mold cap 64. (Figure 10E).

Figures 11A to 11F illustrate another method of producing the present invention. Instead of placing the die directly onto the adhesive layer, semiconductor wafers are adhered to a transition medium and then processed to produce sandwiches 66. This process provides more accurate alignment between die 58 and transition medium 56 when mounted on tape carrier 50. In comparison, the techniques of Figures 9A to 9F require more careful alignment of the structures. The transition material needs to be aligned and placed in the package and the die needs to be aligned and placed on the transition medium. The techniques of Figure 11A to 11F does not require as many or as precise alignment steps. In fact, the assembly of the die and transition material combination can be performed in the same way or is done with a single die. As shown in Figures 11A and 11B, semiconductor wafer 68 is adhered to a transition medium 70 with an adhesive layer 60 to form combination 72. Wafer 68 can be any size or shape, but is typically a circular wafer having a diameter between approximately 6 inches and 12 inches. Wafer 68 typically has a thickness between approximately 18 mils and 30 mils, but can be thinned with plasma etching or lapping to provide any desired thickness. In one embodiment, transition medium 56 length L_{TM} and width W_{TM} are at least as long and wide as the semiconductor wafer 68 length L_D and width W_D . In other embodiments, transition medium 70 can be larger or smaller than wafer 68. After wafer-transition medium combination 72 has been set, it is cut into pieces, as shown by lines 74 of Figure 11B to form the sandwiches 66. The exact size and shape of each sandwich 66 will depend on the desired application. The cutting can be done by any conventional means such as mechanical sawing, laser sawing, punching (shearing), or the like. A second layer of adhesive 54 is placed on the tape carrier 50 (Figure 11C). As illustrated in Figures 11D and 11E, the sandwich 66 is then placed on the adhesive layer 54. Bonding wires 62 can be attached to pads or other features of die 58 to electrically connect the die to appropriate locations on tape carrier 50. Die 58 can then be encased or encapsulated using mold cap 64 (Figure 11F).

In yet another method shown in Figures 12A to 12C, a pre-molded pedestal 56 can be integrally formed on the substrate 50. The die 58 can be positioned directly on the pedestal 56 with or without an adhesive. Thereafter, the mold encapsulate 64 can be placed over the pedestal 56 and the die 58 to seal the integrated circuit. In most embodiments the pre-molded pedestal is comprised of the same material as the mold

encapsulate, however, in other embodiments, the pre-molded pedestal can be other materials which have similar CTE's as the molding compound.

5 This description of embodiments of the invention is presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications. This description of embodiments will enable others skilled in the art to best utilize and practice the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

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WHAT IS CLAIMED IS:

- 1 1. An integrated circuit package comprising:
2 a silicon die having a first thickness;
3 a metallized polymer layer having a first side and a second side; and
4 a transition medium disposed between the silicon die and the first side of
5 the metallized polymer layer wherein the transition medium has a second thickness, and
6 the first thickness of the silicon die is less than the second thickness.
- 1 2. The integrated circuit package of claim 1 wherein the transition
2 medium is nonconductive.
- 1 3. The integrated circuit package of claim 1 comprising a plastic
2 encapsulant which encapsulates the silicon die and the transition medium, the plastic
3 encapsulant having a coefficient of thermal expansion between approximately
4 $7 \times 10^{-6}/^{\circ}\text{C}$ and $15 \times 10^{-6}/^{\circ}\text{C}$.
- 1 4. The integrated circuit package of claim 1 wherein the transition
2 medium comprises a mold compound material, a BT resin compound, a FR-4 compound,
3 or a FR-5 resin compound.
- 1 5. The integrated circuit package of claim 1 wherein the transition
2 medium has a coefficient of thermal expansion between approximately $7 \times 10^{-6}/^{\circ}\text{C}$ and
3 $17 \times 10^{-6}/^{\circ}\text{C}$.
- 1 6. The integrated circuit package of claim 1 wherein the presence of
2 the transition medium reduces stress and fracture damage to the silicon die.
- 1 7. The integrated circuit package of claim 1 wherein a thickness of
2 the metallized polymer layer and a thickness of the plastic encapsulant define a package
3 thickness, wherein the silicon die is disposed near the middle of the package thickness.
- 1 8. The integrated circuit package of claim 7 wherein the package
2 thickness is approximately 0.060 inches or less.
- 1 9. The integrated circuit package of claim 5 wherein the silicon die
2 thickness is less than approximately 6 mils.

1 11. The integrated circuit package of claim 1 wherein a coefficient of
2 thermal expansion for the adhesive is approximately $58 \times 10^{-6}/^{\circ}\text{C}$.

1 12. The integrated circuit package of claim 1 wherein the integrated
2 circuit metallized polymer layer is a tape carrier having a dielectric layer and a conductive
3 layer.

1 13. The integrated circuit package of claim 12 comprising solder balls
2 mounted to the second side of the metallized polymer layer, the solder balls electrically
3 contacting an etched circuit in a conductive layer of the tape carrier.

1 14. The integrated circuit package of claim 13 wherein the solder balls
2 electrically connect the integrated circuit package to a printed circuit board.

1 15. The integrated circuit package of claim 14 wherein the solder balls
2 are arranged in a grid fashion underneath the position for the silicon die.

1 16. The integrated circuit package of claim 1 wherein the cross
2 sectional area of the silicon die is substantially less than or equal to the cross sectional
3 area of the rigid transition medium.

1 17. The integrated circuit package of claim 1 wherein the cross
2 sectional area of the silicon die is larger than the cross sectional area of the transition
3 medium.

1 18. The integrated circuit package of claim 1 wherein the package is a
2 BGA package.

1 19. The integrated circuit package of claim 1 wherein a volume of the
2 silicon die is less than the volume of the rigid transition medium.

1 20. An integrated circuit package comprising:
2 a metallized polymer layer defining a first thickness;
3 a transition medium coupled to the metallized polymer layer;

4 a die coupled to the transition medium; and
5 a mold cap encapsulating the transition medium and the die, the mold cap
6 defining a second thickness, wherein the first thickness and second thickness define a
7 package thickness, wherein the die is disposed near the middle of the package thickness.

1 21. The integrated circuit package of claim 20 wherein the mold cap
2 has a coefficient of thermal expansion similar to a coefficient of thermal expansion of the
3 transition medium.

1 22. The integrated circuit package of claim 20 wherein the die is
2 mounted to the transition medium with a layer of adhesive.

1 23. The integrated circuit package of claim 20 wherein the transition
2 medium comprises a mold cap material, a second layer of adhesive, an elastomer, a BT
3 resin compound, a FR-4 compound, or a FR-5 resin compound.

1 24. The integrated circuit package of claim 20 wherein the metallized
2 polymer layer is a tape carrier.

1 25. An integrated circuit package comprising:
2 a tape carrier;
3 a first adhesive layer disposed on the tape carrier, the first adhesive layer
4 having a coefficient of thermal expansion;
5 a transition medium having a first surface and a second surface, wherein
6 the first surface of the transition medium engages the first adhesive layer, the transition
7 medium having a coefficient of thermal expansion;
8 a second adhesive layer disposed on the second surface of the transition
9 medium, the second layer of adhesive having a coefficient of thermal expansion; and
10 a die disposed on the second adhesive layer; and
11 a mold cap encapsulating the first adhesive layer, the transition medium,
12 the second adhesive layer and the die, wherein the mold cap and tape carrier define a
13 package thickness, wherein the transition medium and the mold cap have approximately
14 the same coefficient of thermal expansion so as to reduce the thermal stress on the die
15 during thermal cycling.

1 26. A method of packaging an integrated circuit comprising:

2 providing a silicon die adhered to a rigid transition medium;
3 applying a layer of adhesive to a tape carrier;
4 mounting the die and transition medium to the adhesive on the tape carrier;
5 and
6 encapsulating the die and transition medium.

1 27. The method of claim 26 comprising electrically connecting the tape
2 carrier to a printed circuit board with a solder ball.

1 28. The method of claim 26 wherein the providing step is carried out
2 by cutting a semiconductor wafer adhered to a transition medium.

1 29. The method of claim 28 wherein the transition medium is
2 approximately the same size and shape of the semiconductor wafer.

1 30. The method of claim 26 further comprising lapping the die to
2 reduce the thickness of the die.

1 31. The method of claim 30 wherein the die is thinner than the
2 transition medium.

1 32. A method of forming an integrated circuit package comprising:
2 providing a metallized polymer layer;
3 attaching a rigid transition medium layer to the metallized polymer layer
4 using a first adhesive layer; and
5 coupling an integrated circuit die to the rigid transition medium using a
6 second adhesive layer.

1 33. The method of claim 32 wherein attaching step is carried out with a
2 material comprising mold compound, BT resin, FR-4 resin, or FR-5 resin.

1 34. The method of claim 32 wherein the attaching step is carried out
2 with a rigid transition medium having a thickness between about 4 mils to about 8 mils.

1 35. A method of fabricating an integrated circuit comprising:
2 providing a semiconductor wafer;

3 attaching the semiconductor wafer to a transition medium using a first
4 adhesive;
5 cutting a die from the semiconductor wafer, wherein the die is attached to
6 a corresponding area of the transition medium; and
7 mounting the die and transition medium to a tape carrier.

1 36. The method of claim 35 wherein the cutting step is carried out by
2 mechanical sawing, laser sawing, punching, or shearing.

1 37. The method of claim 35 comprising lapping the semiconductor
2 wafer prior to the cutting step.

1 38. The method of claim 37 wherein the die thickness is reduced to less
2 than approximately 6 mils.

1 39. The method of claim 35 wherein the attaching step is carried out
2 with a transition medium having a coefficient of thermal expansion between about
3 $7 \times 10^{-6}/^{\circ}\text{C}$ and $17 \times 10^{-6}/^{\circ}\text{C}$.

1 40. The method of claim 35 wherein the attaching step is carried out
2 with a rigid transition medium having a thickness between about 2 mils and 8 mils.

1 41. The method of claim 35 wherein the transition medium comprises a
2 mold compound material, a BT resin compound, a FR-4 resin compound, or FR-5 resin
3 compound.

1 42. The method of claim 35 wherein the thickness of the die, adhesive
2 and transition medium is less than approximately 18 mils.

1 43. The method of claim 35 wherein a coefficient of thermal expansion
2 for the adhesive is about $58 \times 10^{-6}/^{\circ}\text{C}$.

1 44. A method of forming an integrated circuit package comprising:
2 providing a tape carrier;
3 providing a silicon die; and

4 reducing a thermal mismatch stress between the die and the integrated
5 circuit package by disposing a rigid transition medium between the tape carrier and the
6 silicon die.

1 45. A method of forming a package comprising:
2 placing a die on a pre-formed pedestal on a substrate; and
3 encapsulating the die and pedestal with a mold compound.

1 46. The method of claim 45 wherein the pre-formed pedestal
2 comprises the same material as the mold compound.

1 47. The method of claim 45 wherein the placing step is performed
2 without an adhesive.

1 48. The method of claim 45 wherein the pre-formed pedestal and the
2 mold compound have a similar CTE.

METHOD AND STRUCTURE FOR INTEGRATED CIRCUIT PACKAGE

ABSTRACT OF THE DISCLOSURE

5 An integrated circuit package is constructed to potential reduce stress and damage to an integrated circuit die. A rigid transition medium (220) is attached using adhesive layers (215, 42) and interfaces between a tape carrier (260) and the integrated circuit die (210). The integrated circuit package prevents damage such as die cracks and also enhances the service life of the packaged integrated circuit part.

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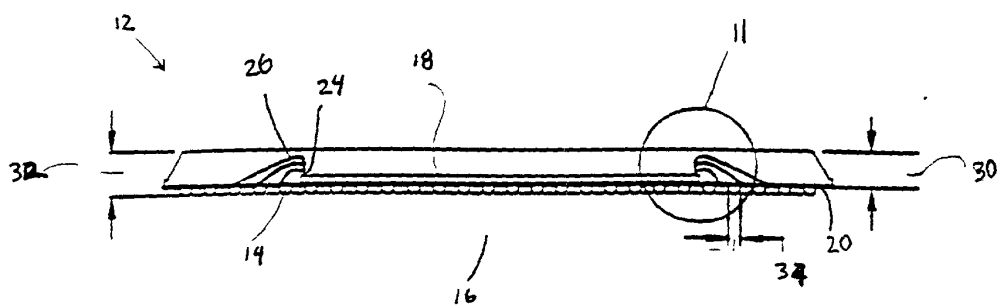


FIG. 1

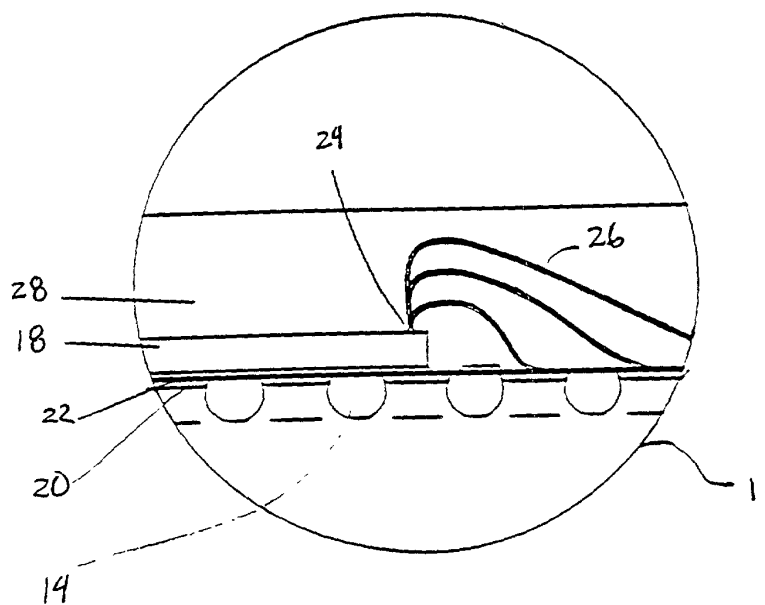


FIG. 2

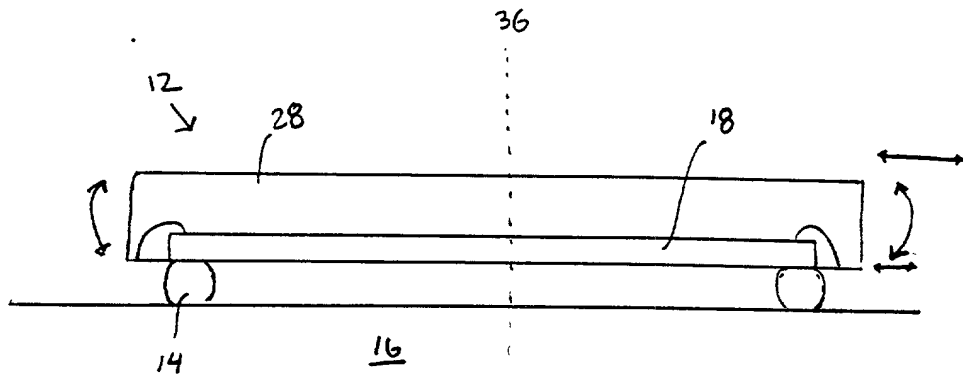


FIG. 3

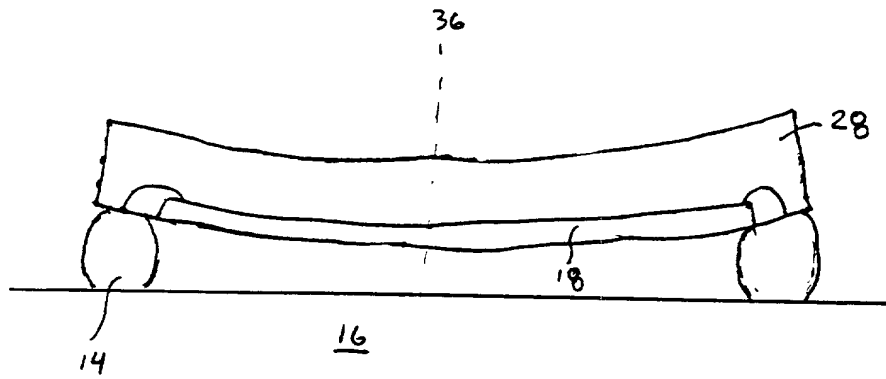


FIG. 4

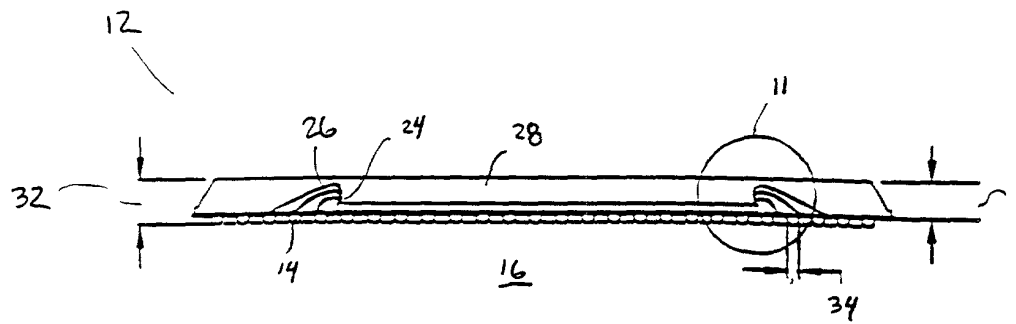


FIG. 5

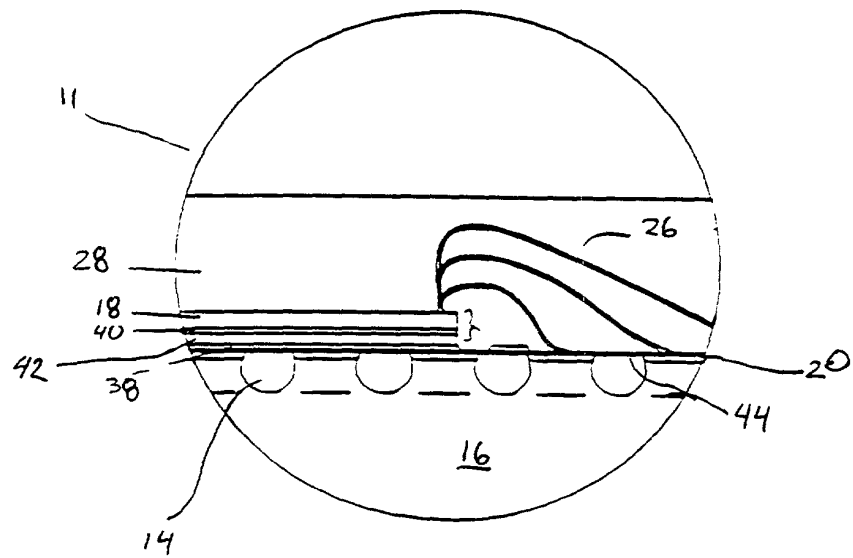


FIG. 6

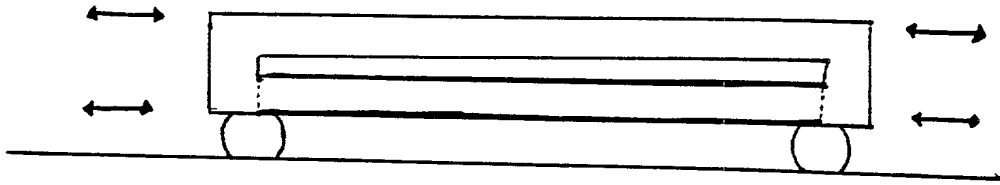


FIG. 7

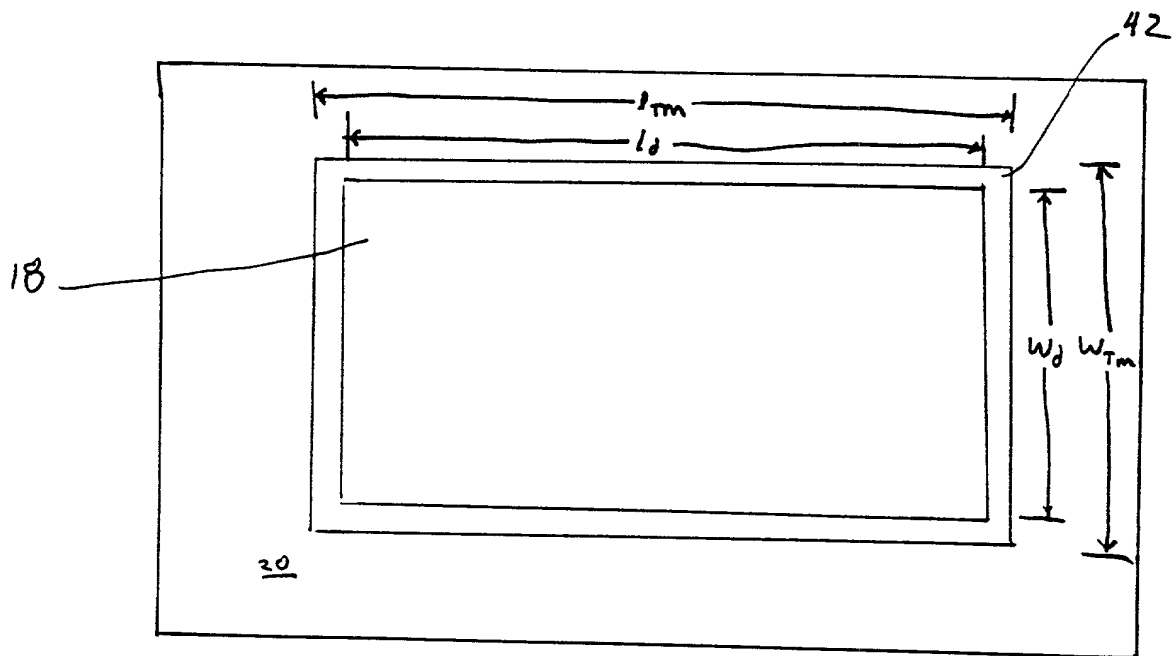
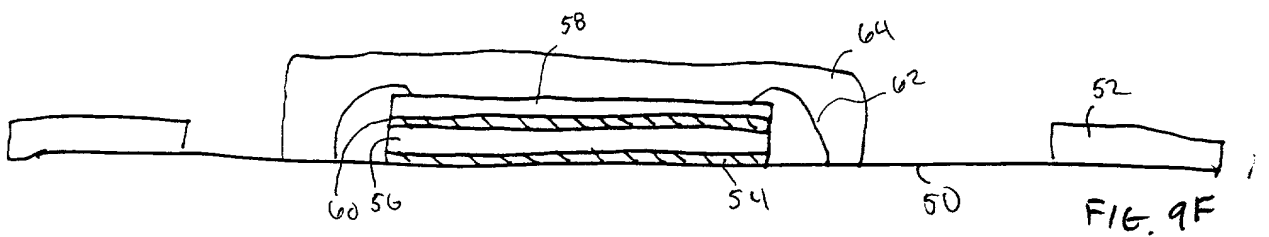
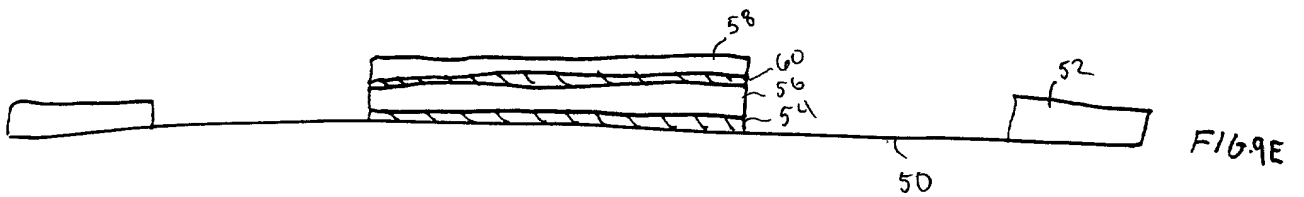
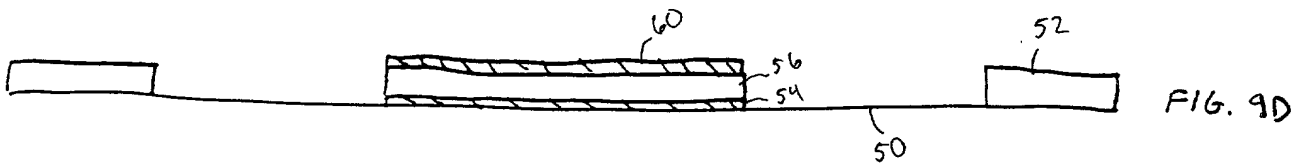
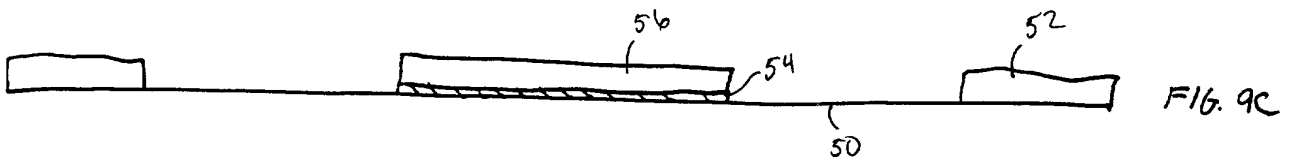
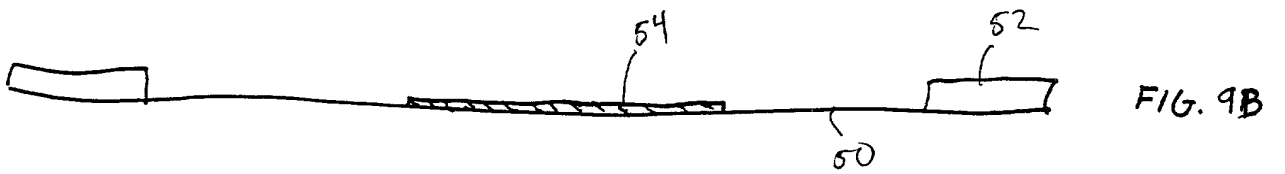
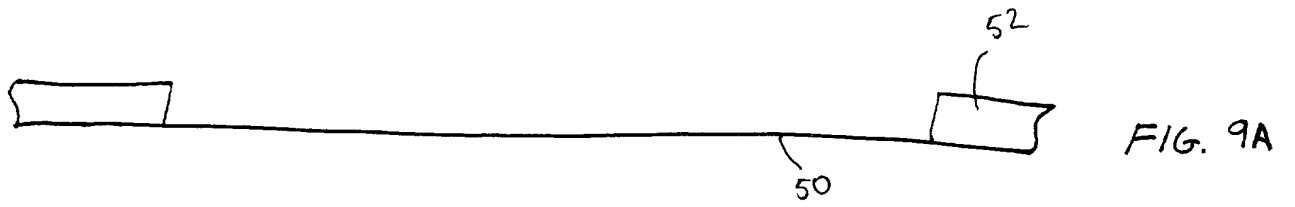


FIG. 8



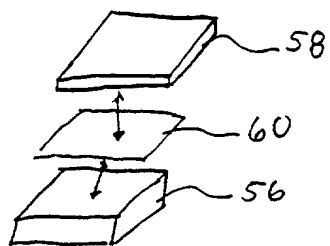


FIG. 10A



FIG. 10B

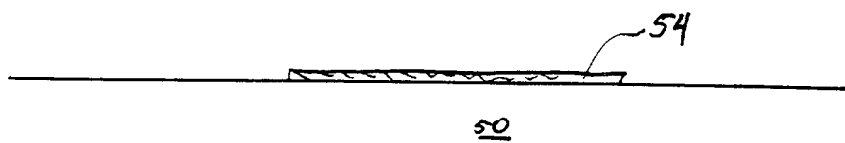


FIG. 10C

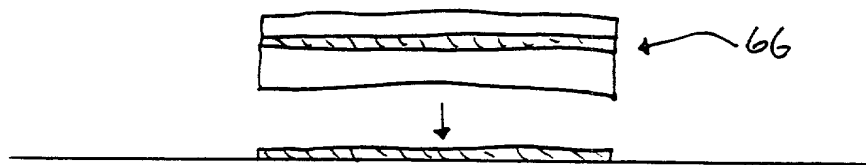


FIG. 10D

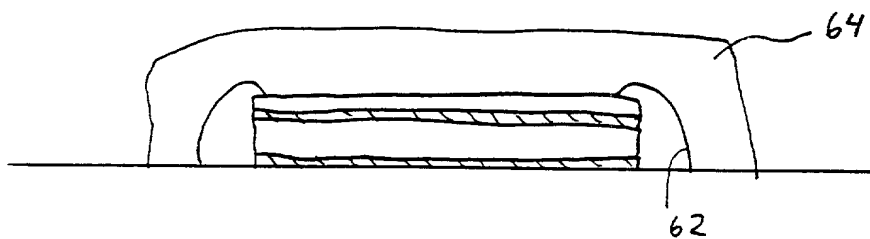


FIG. 10E

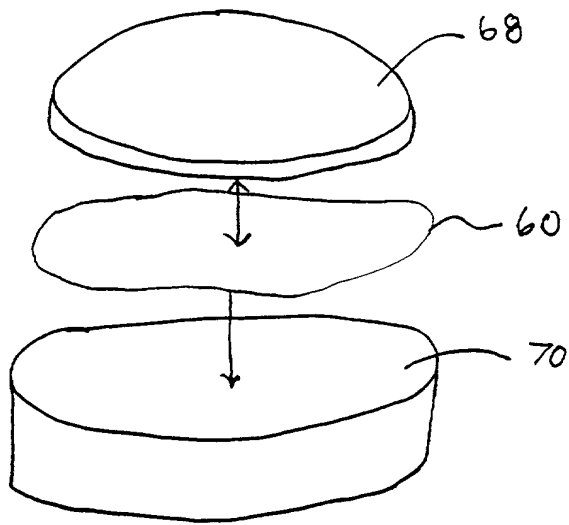


FIG. 11A

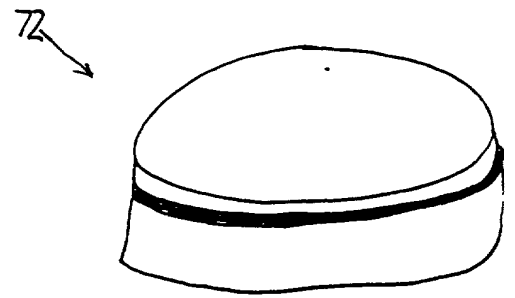


FIG. 11B

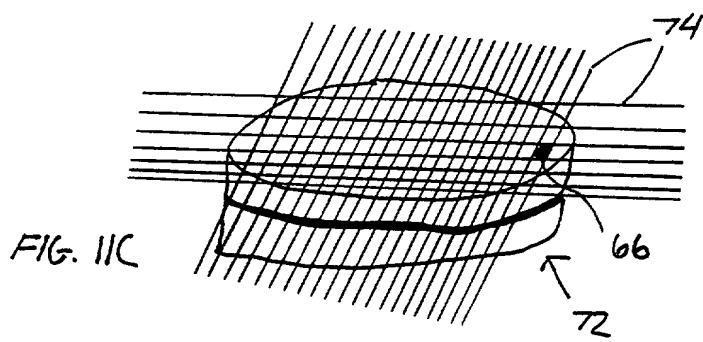


FIG. 11C

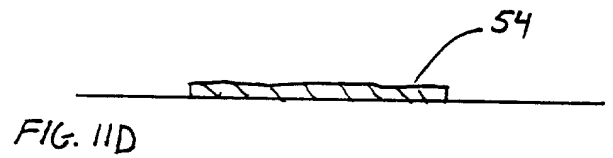


FIG. 11D

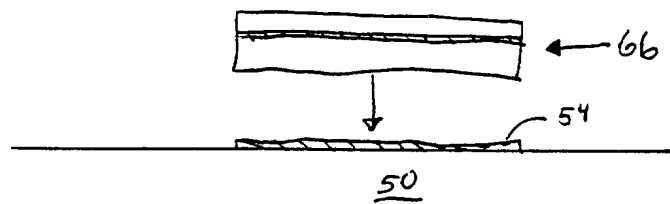


FIG. 11E

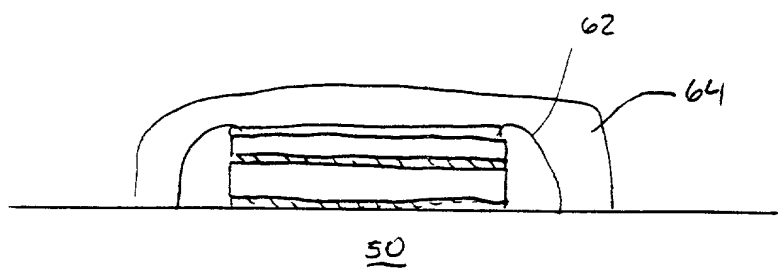


FIG. 11F

FIG. 12A



FIG. 12B

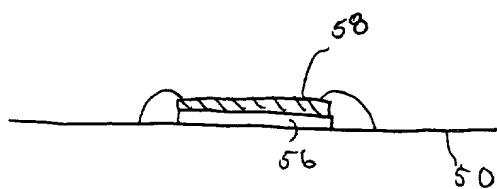
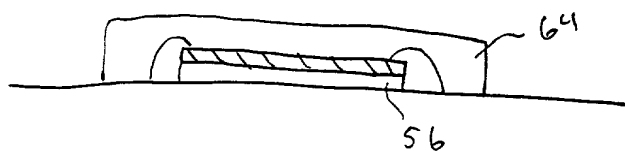


FIG. 12C



DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **METHOD AND STRUCTURE FOR INTEGRATED CIRCUIT PACKAGE** the specification of which X is attached hereto or _____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).


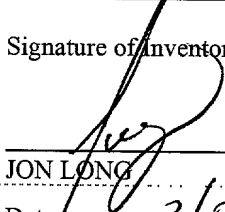

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/123,116	March 5, 1999
60/126,234	March 24, 1999

Full Name of Inventor 1:	Last Name: ANDERSON	First Name: SIDNEY	Middle Name or Initial: LARRY
Residence & Citizenship:	City: Fremont	State/Foreign Country: California	Country of Citizenship: United States
Post Office Address:	Post Office Address: 42991 Luzon Drive	City: Fremont	State/Country: California Postal Code: 94539
Full Name of Inventor 2:	Last Name: LONG	First Name: JON	Middle Name or Initial:
Residence & Citizenship:	City: Livermore	State/Foreign Country: California	Country of Citizenship: United States
Post Office Address:	Post Office Address: 256 Helen Way	City: Livermore	State/Country: California Postal Code: 94550
Full Name of Inventor 3:	Last Name: FRITZ	First Name: DONALD	Middle Name or Initial: S.
Residence & Citizenship:	City: San Jose	State/Foreign Country: California	Country of Citizenship: United States
Post Office Address:	Post Office Address: 5105 Southwick Court	City: San Jose	State/Country: California Postal Code: 95136

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  SIDNEY LARRY ANDERSON Date <u>2/29/00</u>	Signature of Inventor 2  JON LONG Date <u>2/29/00</u>	Signature of Inventor 3  DONALD S. FRITZ Date <u>2/29/00</u>
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POWER OF ATTORNEY BY ASSIGNEE

Altera Corporation is the Assignee of the invention entitled: METHOD AND STRUCTURE FOR INTEGRATED CIRCUIT PACKAGE, the specification of which X is attached hereto or _____ was filed on _____ as Application No. _____.

Assignee hereby appoints the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Paul C. Haughey, Reg. No. 31,836
Derek E. Miniham, Reg. No. 39,774
Charles J. Kulas, Reg. No. 35,809
Babak S. Sani, Reg. No. 37,495
Melvin D. Chan, Reg. No. 39,626
Craig P. Wong, Reg. No. 45,231
Gregory S. Bishop, Reg. No. 41,621
Sujit B. Kotwal, Reg. No. 43,336

Send Correspondence to:

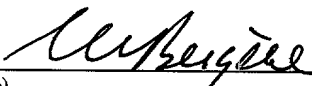
Paul C. Haughey
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834

Direct Telephone Calls to:
(Name, reg. no., tele. no.)

Melvin D. Chan
Reg. No.: 39,626
(650) 326-2400

Altera Corporation
101 Innovation Drive
San Jose, CA 95134

Date: 2/29/2000

By: 
(Signature)

Name: C. Wendell BERGERE

Title: VICE President, General Counsel and Secretary